IN THE CLAIMS:

1. (Currently Amended) A tracing system, comprising:

an embedded processor, said embedded processor including,

a processor core for executing instructions; and

trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with a synchronization period defined by at least a part of a trace control register;

wherein said trace control register includes fields to specify an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information.

2. (Original) The tracing system of claim 1, wherein said synchronization period enables multiple instances of said periodically generated trace synchronization information to be stored at one time in a trace memory.

3. (Original) The tracing system of claim 2, wherein said embedded processor includes said trace memory.

4. (Original) The tracing system of claim 2, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic.

5. (Original) The tracing system of claim 4, wherein said trace capture block sends trace data to an off-chip trace memory.

6. (Original) The tracing system of claim 1, wherein said synchronization period is defined by a single field in said trace control register.

7. (Original) The tracing system of claim 6, wherein bit values contained in said single field correspond to predefined synchronization periods.

8. (Original) The tracing system of claim 7, wherein a first set of said predefined synchronization periods apply to an on-chip implementation of said trace memory, and a second set of said predefined synchronization periods apply to an off-chip implementation of said trace memory.

9. (Original) The tracing system of claim 1, wherein said trace synchronization information includes program counter information.

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Original) A tracing method, comprising:

periodically generating trace synchronization information in accordance with a predefined synchronization period, said trace synchronization information including program counter information and information that enables a determination of a characteristic of an operating state of a processor; and

outputting said trace synchronization information to a trace memory.

14. (Original) The tracing method of claim 13, wherein said characteristic is an operating mode of said processor.

15. (Original) The tracing method of claim 14, wherein said operating mode is one of a kernel mode, a supervisor mode, a user mode, and a debug mode.

16. (Original) The tracing method of claim 13, wherein said characteristic identifies a current process being executed by said processor.

17. (Original) The tracing method of claim 16, wherein said characteristic includes application space identity information.

18. (Original) The tracing method of claim 13, wherein said periodically generated synchronization information includes load and store address information.

19. (Currently Amended) A computer program product comprising:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with a synchronization period defined by at least a part of a trace control register;

wherein said trace control register includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information; and

a computer-usable medium configured to store the computer-readable program codes.

20. (Currently Amended) A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with a synchronization period defined by at least a part of a trace control register;

wherein said trace control register includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information.

21. (Currently Amended) A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with a synchronization period defined by at least a part of a trace control register;

wherein said trace control register includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information..

22. (Original) The method of claim 21, wherein computer-readable program code is transmitted to said computer over the Internet.